Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(routing adj resources) and ((test adj (design or circuit)) same (PLD or FPGA)) and (nets same sources same loads)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/13 15:44
S1	956	716/12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 13:25
S2	666	716/16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 13:23
S3	750	716/17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 13:23
S4	0	(716/12).ccls. and (target adj (rout$ adj resource))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 13:27
S5	0	(716/16).ccls. and (target adj (rout$ adj resource))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 13:27
S6	0	(716/17).ccls. and (target adj (rout$ adj resource))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 13:27
S7	1	("716"/$).ccls. and (target adj (rout$ adj resource))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 13:28
S8	1	(target adj (rout$ adj resource))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 13:29
S9	7	(PLD or FPGA) and (test adj design) and (rout$ adj resource)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 14:25

S10	6148	(PLD or FPGA) and ((rout$ adj resource) same target same source samd load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 14:27
S11	0	(PLD or FPGA) and ((rout$ adj resource) same target same (source same load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 14:27
S12	0	(PLD or FPGA) and ((rout$ adj resource) same (source same load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 14:28
S13	37	(PLD or FPGA) and ((test design) same (rout$ adj resource))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 14:51
S14	37	(PGA or PLD or FPGA) and ((test design) same (rout$ adj resource))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 16:50
S15	0	(PGA or PLD or FPGA) and ((rout$ adj resource) same source same load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:01
S16	0	(PGA or PLD or FPGA) and ((rout$ adj resource) same (start$) same (load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:00
S17	0	(PGA or PLD or FPGA) and ((rout$ adj resources) same (start$) same (load))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:01
S18	15	(PGA or PLD or FPGA) and ((rout$ adj resources) same source same load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:06
S19	2	(PGA or PLD or FPGA) and (rout$ adj resources) and (router same source same load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:15

S20	6	(rout$ adj resources) and (router same source same load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:18
S21	2	(routing adj resources) and (router same source same load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:21
S22	0	(testing adj (routing adj resources)) and (source same load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:22
S23	4	(testing same (routing adj resources)) and (source same load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:39
S24	66	(testing same (routing adj resources))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 17:39
S25	16	(PGA or PLD or FPGA) and (testing same (rout$ adj resource))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 18:02
S26	0	(PGA or PLD or FPGA) and (testing same (rout$ adj resource)) and (forward$ and backward$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 18:03
S27	0	(PGA or PLD or FPGA) and (rout$ adj resources) and ((rout$ adj forwards) or (rout$ adj backwards))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/08 18:05
S28	50	(routing adj resources) and (test adj (design or circuit)) and (PLD or FPGA)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/13 14:51
S29	14	(routing adj resources) and (test adj (design or circuit)) and (PLD or FPGA) and (nets and start$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/13 14:31

S30	0	(routing adj resources) and (test adj (design or circuit)) and (PLD or FPGA) and (nets same (start or beginning) same (load or end))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/13 14:33
S31	25	(routing adj resources) and ((test adj (design or circuit)) same (PLD or FPGA))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/13 15:43

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